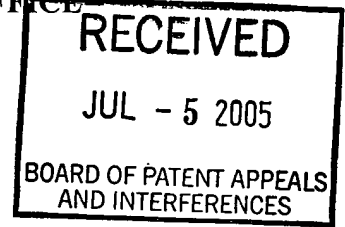


**DOCKET NO. 94-C-096C4 (STMI01-94096)**  
**Customer No. 30425**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: : KUEI-WU HUANG ET AL  
Serial No. : 09/517,987  
Filed : March 3, 2000  
For : METHOD OF FORMING PLANARIZED STRUCTURES  
IN AN INTEGRATED CIRCUIT  
Group No. : 2812  
Examiner : R. Booth



**MAIL STOP APPEAL BRIEF - PATENTS**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

**REQUEST FOR RECONSIDERATION OF DECISION ON APPEAL**

Pursuant to 37 C.F.R. § 41.52, Appellants respectfully request reconsideration of the Decision On Appeal mailed April 29, 2005 ("Decision").

**1. Hsu provides no basis for the conclusions drawn in the Decision**

As previously noted, in the present invention, the source/drain regions are "wrapped" around the gate by formation of the raised source/drain portions, so that shallow source/drain regions implanted within the substrate may be augmented by the raised source/drain regions. As also previously noted, source and drain regions are understood by those in the art to be regions in which charge carrier (electron or hole) generation or recombination occur. See, e.g., US 5,198,379, column

1, lines 37–39; US 4,408,304, column 8, lines 23–25. Conductive structures connected to the source and drain regions, such as metal contacts or interconnects, do not provide charge carrier generation or recombination, but instead merely provide conduction or movement of such charge carriers generated or recombined elsewhere, to provide current flow.

The Decision states:

In affirming the rejection of the claims on appeal, we do not agree with any of arguments [sic] presented by appellants in the brief and reply brief because the summary of the invention, taken as a whole, clearly indicates the position of the examiner is correct. For example, topic (b) at column 1, lines 53 through 54 states:

(b) forming the source and drain regions adjacent the side walls of the gate so that the regions extend downwardly from the surface to a depth of less than 100 nm.

Appellants' consideration of the specific teaching at columns 2 and 3 of Hsu presents an incomplete consideration of the teachings of this reference.

Decision at page 5. However, in making this statement, the Decision itself employs only an “incomplete consideration of the teachings” of *Hsu*, inferentially draws conclusions not supported by the teachings in the reference, and fails to identify what specific teachings in *Hsu* are not reflected in the arguments presented by Appellants.

The portion of *Hsu* cited in the above quote, taken in context, actually reads:

According to the present invention, a MOSFET device and method of making is disclosed. The FET includes a surface, an insulated gate formed on the surface, and source and drain regions formed adjacent the side walls of the gate and extending downwardly from the surface to a depth of less than 100 nm. The method includes the steps:

(a) forming the insulated gate;

(b) forming the source and drain regions adjacent the side walls of the gate so that the regions extend downwardly from the surface to a depth of less than 100 nm;

(c) forming a protective layer over the entire gate;

(d) forming a layer of single crystalline silicon on the surfaces of the source and drain regions;

(e) doping the silicon layer to a depth about equal to its thickness; and

(f) forming a layer of metal silicide on the silicon layer.

*Hsu*, column 1, lines 44–61. Step (b) above relates to formation of regions 24 and 26, while steps (d) and (e) relate to formation and doping of epitaxial layer 50. Thus, the “source and drain regions” described in step (b) do NOT include the doped epitaxial layer 50.<sup>1</sup> The Decision’s selective reading of only a portion of the summary is therefore improper. *Hsu*, taken as a whole, does NOT teach forming raised source and drain regions over the implanted source and drain regions and adjacent the insulating material on the sides of the gate electrode as recited in the claims.

The Decision also states:

The examiner’s responsive arguments at pages 5 and 6 of the answer take the view that *Hsu* teaches the same structure as appellants have disclosed, citing figure 5a and region 40 shown in appellants’ specification drawings. The examiner’s view concludes that because the epitaxial regions 50 of *Hsu* and the source/drain regions 24 and 26 in the substrate are in electrical contact with each other, they must necessarily function together as source and drain regions.

Decision, page 5. To the extent the Decision inherently approves such reasoning, there is no evidence of record that supports the conclusion or inference stated. In fact, the conclusion is contrary

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<sup>1</sup> “Adjacent” in step (b) does not mean that the source and drain regions are formed alongside or next to the gate electrode as implied in the Decision, but instead merely that they are formed within the portion of the substrate adjacent to that over which the gate electrode is formed.

to the evidence of record. First, *Hsu* teaches that the epitaxial layer regions 50 are heavily doped (N+), which indicates that those regions are mere conductive structures similar to conductive plugs 38, 40 in *Pierce*, which *Pierce* teaches may also be formed of heavily doped single-crystal silicon (or doped polysilicon, or metal). *Pierce*, column 11, lines 12–59. The “highly doped” epitaxial regions 50 in *Hsu* thus differ from the structure disclosed in Appellants’ specification by being heavily doped conductive structures, rather than normally doped semiconductor regions that may function as source or drain regions for charge carrier generation or recombination. Second, *Hsu* states that the completed structure disclosed has shallow source and drain regions having a depth of only 100 nm or less:

The important advantage of the present invention is that a very low sheet resistance is obtained for shallow source and drain regions having a depth of only 100 nm or less.

*Hsu*, column 3, lines 44–47. That “100 nm or less” depth is the same depth to which regions 24, 26 are implanted into the substrate. *Hsu*, column 2, lines 31–33, column 1, lines 47–49 and 52–54. Thus, the only portions of the structure disclosed in *Hsu* that function as a source or drain region are the implanted regions 24, 26, and NOT the heavily doped epitaxial regions 50 formed over the implanted regions 24, 26. Indeed, a principal object of *Hsu* is to form source and drain regions 24, 26 that are sufficiently shallow to prevent punch-through. *Hsu*, column 1, lines 9–41. Therefore, by *Hsu*’s own teachings, the heavily doped epitaxial regions 50 do not form part of the source and drain for the transistor disclosed therein, and do not satisfy the claim limitation at issue.

Finally, the Decision states that Appellants' presentation of *Hsu* is "an incomplete consideration of the teachings" of that reference. However, the Decision identifies no portion – other than step (b), taken out of context in the Decision as shown above – of the *Hsu* teachings that Appellants have overlooked.

2. **The limitation "lightly doped" is not satisfied by merely being less heavily doped than another region.**

Appellants' brief noted that claims 87 and 90 recite that the portions of the source and drain regions within the substrate comprise light-doped source and drain regions for the transistor. The Decision states:

To the extent dependent claims 87 and 90 are argued by appellants at page 13 of the principal brief on appeal, the figures in *Hsu* show that the respective source and drain regions 24 and 26 in the substrate have a doping level of N, whereas the upward, extended regions of the source and drain regions adjacent to the gate electrode are represented by N<sup>+</sup>, thus indicating respective light dopings and comparatively heavier doping levels.

Decision, page 6. However, the mere fact that the implanted source and drain regions 24, 26 in *Hsu* are "comparatively" less heavily doped than the heavily doped epitaxial regions 50 does NOT make those regions "lightly doped" regions within the ordinary meaning of that term.

3. **The Decision completely ignores Appellants' arguments regarding claim 93.**

Appellants' brief also noted that independent claim 93 recites that the insulating material on both the bottom and the sides of the gate electrode form a gate oxide between the gate electrode and the source/drain regions. As noted, *Hsu* contains no teaching that the oxide on the side walls 28 of

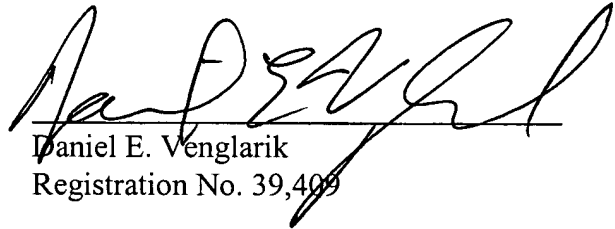
gate electrode 20 functions as a gate oxide. The Decision completely ignores this claim and argument, and is therefore arbitrary and capricious.

Because of the above-identified errors in the Decision, Applicant respectfully requests reconsideration of the Decision and reversal of the decision of the Examiner below rejecting pending claims 77-96 in this application.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: 6-29-05

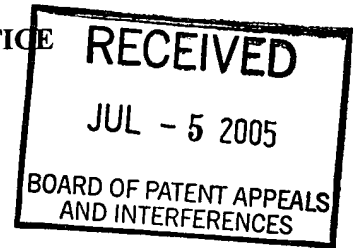
  
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PATENT

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In re application of: : KUEI-WU HUANG ET AL  
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Examiner : R. Booth

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Sir:

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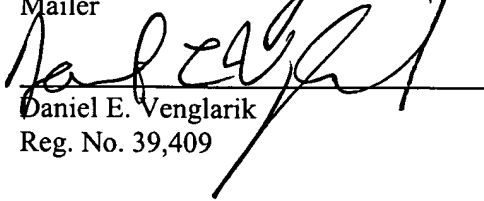
1. Request for Reconsideration of Decision on Appeal; and
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relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to Board of Patent Appeals and Interferences, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, on June 29, 2005.

Date: 6-29-05

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